UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P O Box 1450
Alexandria, Virginia 22313-1450
www uspto gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/715,459	11/19/2003	Curtis Davis	NVDA/AG-08-0112-US	3916

26290 7590 10/09/2009
PATTERSON & SHERIDAN, L.L.P.
3040 POST OAK BOULEVARD
SUITE 1500
HOUSTON, TX 77056

EXAMINER	
VICARY, KEITH E	

ART UNIT	PAPER NUMBER
2183	

MAIL DATE	DELIVERY MODE
10/09/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/715,459	DAVIS ET AL.	
	Examiner	Art Unit	
	Keith Vicary	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 July 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5,7,10-17 and 19-40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,7,10-17 and 19-40* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *5/20/2009*.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application

6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-5, 7, 10-17, and 19-40 are pending in this office action and presented for examination. Claims 10, 14, 19, 31, and 38-40 are newly amended by amendment filed 7/9/2009.

Double Patenting

2. Claims 1-5, 7, 10-14, 16, 22-23, 25, 31-35, and 38-40 of this application conflict with claims 1, 2, 5, 7-8, 15, 20, 23, 27, and 30 of Application No. 10715370. 37 CFR 1.78(b) provides that when two or more applications filed by the same applicant contain conflicting claims, elimination of such claims from all but one application may be required in the absence of good and sufficient reason for their retention during pendency in more than one application. Applicant is required to either cancel the conflicting claims from all but one application or maintain a clear line of demarcation between the applications. See MPEP § 822.

3. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to

be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

4. Claims 1-5, 7, 9-14, 16, 18, 22-23, 25, 31-35, and 38-40 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1, 2, 5, 7-8, 15, 20, 23, 27, and 30 of copending Application No. 10715370. Although the conflicting claims are not identical, they are not patentably distinct from each other because each particular instant claim is an obvious variant of the corresponding claim of the '370 application.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

5. All limitations of claim 1 of the instant application are taught in claim 1 of the '370 application except the one or more peripherals; however, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine a peripheral with the instant claim in order to, for example, interact with the CPU.

a. All further limitations of claim 2 of the instant application are also taught in claim 1 of the '370 application.

b. All further limitations of claim 3 of the instant application are also taught in claim 1 of the '370 application.

c. All further limitations of claim 4 of the instant application are also taught in claim 8 (dependent on claim 1) of the '370 application.

d. All further limitations of claim 5 of the instant application are taught in claim 2 (dependent on claim 1) of the '370 application.

e. All further limitations of claim 7 of the instant application are taught in claim 5 (dependent on claim 1) of the '370 application except that the PCE comprises programming code; however, it would have been obvious to one of ordinary skill in the art at the time of the invention that an engine can be implemented as either software or hardware.

f. All further limitations of claim 10 of the instant application are taught in claim 5 (dependent on claim 1) of the '370 application except that the PPM is high-speed and is connected to one of the DME and the FPE by a high-speed data bus; however, it would have been obvious to one of ordinary skill in the art at the time of the invention that a high-speed memory would lead to greater system performance, that a data bus would be able to be used to connect two components, and that the data bus being high-speed would also lead to greater system performance.

g. All further limitations of claim 11 of the instant application are taught in claim 5 (dependent on claim 1) of the '370 application, as some form of memory interface is inherent given a memory connected to a data bus.

h. All further limitations of claim 12-13 of the instant application are taught in claim 5 (dependent on claim 1) of the '370 application, as a PPU operatively connected to a CPU entails some form of connection, and it would have been obvious to one of ordinary skill in the art at the time of the invention for this

connection to be a bus, as well as for a bridge to be used to connect an internal and external bus.

i. All further limitations of claim 14 of the instant application are taught in claim 5 (dependent on claim 1) of the '370 application.

j. All further limitations of claim 16 of the instant application are taught in claim 7 (dependent on claim 1) of the '370 application.

6. All limitations of claim 22 and 23 of the instant application are taught in claim 20 (which is dependent on claims 17 and 18) of the '370 application except for limitations which are obvious variants of claim 20 of the '370 application which are explained above.

7. All limitations of claim 25 of the instant application are taught in claim 15 of the '370 application except for limitations which are obvious variants of claim 15 of the '370 application which are explained above.

8. All limitations of claim 31 of the instant application are taught in claim 23 of the '370 application except for limitations which are obvious variants of claim 23 of the '370 application which are explained above.

9. All further limitations of claims 32 and 33 of the instant application are taught in claim 27 of the '370 application.

10. All further limitations of claims 34 of the instant application are taught in claim 23 of the '370 application.

11. All further limitations of claims 35 of the instant application are taught in claim 30 of the '370 application.

12. Claims 1-5, 7, 10-14, 16, 20, 22-23, 25, 29-36, and 38-40 of this application conflict with claims 2, 8, and 19 of Application No. 10715440. 37 CFR 1.78(b) provides that when two or more applications filed by the same applicant contain conflicting claims, elimination of such claims from all but one application may be required in the absence of good and sufficient reason for their retention during pendency in more than one application. Applicant is required to either cancel the conflicting claims from all but one application or maintain a clear line of demarcation between the applications. See MPEP § 822.

13. Claims 1-5, 7, 10-14, 16, 20, 22-23, 25, 29-36, and 38-40 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 2, 8, and 19 of copending Application No. 10715440. Although the conflicting claims are not identical, they are not patentably distinct from each other because each particular instant claim is an obvious variant of the corresponding claim of the '440 application.

This is a <u>provisional</u> obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

14. The rationale for these rejections are analogous to the rejection using the '370 application above. To summarize:

k. The limitations of claims 1-4 of the instant application are obvious variants of claim 2 of the '440 application.

l. The limitations of claims 10-14, 16, 22-23, 25, and 29-37 of the instant application are obvious variants of claim 19 of the '440 application.

m. The limitations of claim 20 of the instant application are obvious variants of claim 8 of the '440 application.

Claim Rejections - 35 USC § 103

15. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

16. Claims 1-4, 7, 10-17, 19-23, 25-27, 29-31, 34, and 38-40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Van Hook et al. (Van Hook) (US 6342892 B1) in view of Bishop et al. (Bishop) (Sparta: Simulation of Physics on a Real-Time Architecture) in view of Dakhil (US 6341318 B1).

17. Consider claims 1, 25, and 31, Van Hook discloses a Central Processing Unit (CPU) (Figure 2, main processor 100) coupled to an external memory (Figure 2, video game storage device 54) and one or more peripherals (Figure 2, game controllers); and a coprocessor (Figure 2, coprocessor 200) coupled to the CPU (Figure 2, interconnect 102) and a Processing Memory (PM) (Figure 5, memory 300) and comprising a Coprocessor Control Engine (CCE) (Figure 5, signal processor 400 in tandem with CPU interface 202), a Data Movement Engine (DME) (col. 17, lines 17-19, DMA circuit) and a

Calculation Engine (CE) (col. 18, lines 8-18, execution unit 430; alternatively, for example, display processor 500 from col. 16, lines 44-47), wherein the CCE is configured to receive simulation requests from the CPU (col. 7, lines 4-9, main processor generates lists of commands that tell the coprocessor what to do, for graphics and audio simulation; col. 9, lines 1-2, the signal processor, and CPU interface preliminarily, reads these lists; also see col. 8, lines 39-46, commands which control the coprocessor) via a coprocessor software driver executing on the CPU (col. 13, lines 9-16, drivers to manage the various resources of system 50) and to issue commands to the DME (see col. 22, lines 13-15, signal processor retrieves additional SP microcode modules from main memory as needed to perform the specified tasks...may use its DMA facility) and the CE (col. 18, lines 11-13, execution unit is managed by instruction memory 402; col. 19, lines 41-44 discloses that the signal processor can transfer data into and out of instruction memory 402; col. 11, lines 65-67 discloses that the signal processor executes the microcode out of the instruction memory 402; thus it is issuing commands to the execution unit; alternatively, col. 16, lines 44-47, command list for display processor comes directly from signal processor 400) to perform simulation computations associated with the simulation requests (col. 7, lines 4-9, discloses of graphics and audio simulation, as above), the DME is configured to transfer data between the PPM and at least one PPU internal memory in response to commands received from the PCE (col. 22, lines 13-15, signal processor retrieves additional SP microcode modules from main memory as needed to perform the specified tasks...may use its DMA facility; also, col. 19, lines 41-44, DMA controller to transfer data out of

instruction memory and data memory; data memory 404, instruction memory 402), and the CE is configured to respond to commands from at least one of the PCE and the DME and to execute floating point computations on physics data stored in the at least one PPU internal memory (col. 18, lines 11-13, execution unit is managed by instruction memory 402; col. 19, lines 41-44 discloses that the signal processor can transfer data into and out of instruction memory 402 and data memory 404; col. 11, lines 65-67 discloses that the signal processor executes the microcode out of the instruction memory 402; thus it is issuing commands to the execution unit; alternatively, col. 16, lines 44-47, command list for display processor comes directly from signal processor 400; col. 11, line 50, discloses of an internal texture memory into which texture data is copied). With regard to claim 25, Van Hook discloses a host (the above citations of the external memory and a peripheral coupled to a CPU, collectively), wherein the host stores a main game program (col. 4, lines 35-37, video game storage device 54) and the PPU software driver; and, wherein the PPU software driver manages all communication between the PPU and the CPU (col. 13, lines 9-16, drivers to manage the various resources of system 50).

However, Van Hook does not explicitly disclose that the coprocessor is a Physics Processing Unit (PPU), and thus does not disclose that the Processing Memory (PM) is a Physics Processing Memory (PPM), the Coprocessor Control Engine (CCE) is a PPU Control Engine (PPE), the Calculation Engine (CE) is a Floating Point Engine (FPE), the simulation computations are physics simulation computations, the simulation requests

are physics simulation requests, the data is physics data, and the computations on data are floating point computations on physics data.

On the other hand, Bishop does disclose of a Physics Processing Unit for real-time processing of physics simulation data (Figure 1, ideal SPARTA implementation; section 1 discloses of physical modeling of solid objects through the use of specialized hardware; section 2 and section 3.1 discloses of collision detection and force computation).

Bishop's teaching of using specialized hardware accelerates physical models of specialized hardware to achieve real-time performance for creating realistic virtual environments (Bishop, section 1).

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teaching of Bishop with the invention of Van Hook in order to accelerate physical models of specialized hardware to achieve real-time performance for creating realistic virtual environments. Note that Bishop's teaching of using specialized hardware for physics simulation, when applied to the invention of Van Hook, teaches that the Processing Memory (PM) is a Physics Processing Memory (PPM), the Coprocessor Control Engine (CCE) is a PPU Control Engine (PPE), the Calculation Engine (CE) is a Floating Point Engine (FPE), the simulation computations are physics simulation computations, the simulation requests are physics simulation requests, the data is physics data, and the computations on data are floating point computations on physics data.

However, neither Van Hook nor Bishop discloses of initiating context switches relative to one or more banks of the at least one PPU internal memory.

On the other hand, Dakhil does disclose of initiating a context switch relative to one or more banks of at least one data memory (the steps of col. 2, lines 15-44, wherein data is loaded to banks in an interleaved fashion in order to be processed).

Dakhil's teaching increases the efficiency of data processing system by minimizing idle processing iterations (Dakhil, col. 3, lines 24).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teaching of Dakhil with the invention of Van Hook and Bishop in order to increase data processing efficiency by minimizing idle processing iterations.

18. Consider claim 2, Van Hook discloses the CPU comprises a processing unit resident in a personal computer (col. 6, line 51, computer).

19. Consider claim 3, Van Hook discloses the CPU comprises a processing unit resident in a game console (col. 1, lines 13-14, video game systems).

20. Consider claim 4, Van Hook discloses of a Graphics Processing Unit (GPU) operatively connected to the CPU (Figure 2, display processor 500).

21. Consider claim 7, Van Hook discloses the PCE (Figure 5, signal processor 400) comprises programming code stored in a memory resident within the PPU (Figure 5, microcode RAM 402).

22. Consider claim 10, Van Hook discloses that the PPM comprises a high-speed memory and the PPU further comprises a high-speed data bus connecting the high-speed memory to at least one of the DME and the FPE (Figure 5, RDRAM 300, bus 106 explained in col. 15, lines 1-3, Figure 5 also shows data being stored).

23. Consider claim 11, Van Hook discloses a memory interface unit managing data communication between the high- speed data bus and the high-speed memory (Figure 5, DRAM controller/Interface).

24. Consider claim 12, Van Hook discloses a processor bus connecting the PCE with at least one physical interface to the CPU (Figure 5, bus 214).

25. Consider claim 13, Van Hook discloses the processor bus is separate from the high-speed bus and connected to the high-speed bus via a bridge (Figure 5, wherein the dram controller/interface 212 acts as the bridge).

26. Consider claim 14, Van Hook discloses an Inter-Engine Memory (IEM) coupled to the DME and the FPE (Van Hook, Figure 6, instruction memory 402 or data memory

404 is the IEM) and configured to receive physics simulation data from the PPM (Van Hook, col. 19, lines 41-49, DMA controller can copy microcode modules from main memory into signal processor instruction memory, and may also be used to transfer information between data memory and main memory) in response to commands received from the DME (Van Hook, col. 19, line 41-45, DMA controller used to transfer data into and out of instruction memory and/or data memory).

27. Consider claim 15, Van Hook discloses an Inter-Engine Register (IER) coupled to the DME and the FPE and adapted to initiate DME operation in response to a PCE command (see, for example, col. 19, lines 60-67, SP-DRAM DMA address register 458 can be written to from SP execution unit and is used to specify a starting DMA address within instruction memory or data memory; alternatively, the program counter can also read on the inter-engine register; alternatively, a value in a register can initiate a DME operation in that it is that value which is sent using the DME).

28. Consider claim 16, Dakhil disclose the IEM comprises multiple banks of memory adapted to support parallel threads of execution (the steps of col. 2, lines 15-44 as explained in the combination of the independent claim).

29. Consider claim 17, Van Hook discloses the IER comprises multiple registers (col. 18, line 40), and Dakhil discloses the IEM or IER comprises multiple banks of memory

adapted to support two parallel threads of execution (the steps of col. 2, lines 15-44; see the combination above).

30. Consider claim 19, Van Hook discloses a DME control interface comprising: a first packet queue receiving command packets from the PCE and communicating command packets to the DME; and, a second packet queue receiving response packets from the DME and communicating the response packets to the PCE (col. 19, lines 61-67 and col. 20, lines 1-8, data can be both written to and read from the memory; the SP-DRAM DMA address register serves as the first packet queue and the data memory in the signal processor is the second packet queue, or the buffer of col. 61, line 19).

31. Consider claim 20, Van Hook as modified by Dakhil disclose a Scratch Pad Memory (SPM) receiving data from the PPM in response to commands from the DME (Van Hook, Figure 6, instruction memory 402 or data memory 404, see col. 19, lines 41-50), wherein the IEM further comprises a first bank accessible to the DME and a second bank accessible to the FPE (Dakhil, col. 2, lines 15-39 as above); and, wherein the DME further comprises: a first unidirectional crossbar connected to the first bank (Dakhil, col. 2, lines 15-39 as above and col. 4, lines 14-22; the inputs are the external device and the first memory area, the outputs are the banks of the IEM; this crossbar encompasses the read address signals), a second unidirectional crossbar connected to the second bank (Dakhil, col. 2, lines 15-39 as above and col. 4, lines 14-22; the inputs are the banks of the IEM, the outputs are the external device and the first memory area;

this crossbar encompasses the write address signals); and, a bi-directional crossbar connecting first and second crossbars to at least one of the PPM or SPM (Dakhil, col. 2, lines 15-39 as above and col. 4, lines 14-22; the inputs are the data from each bank of the IEM, the outputs are the external device and the first memory area; also see Figure 7 of Van Hook, Register files. Also see col. 15, lines 22-24, communication between components).

32. Consider claim 21, Van Hook as modified by Dakhil disclose a first Address Generation Unit providing Read address data to the first unidirectional crossbar (Dakhil, col. 2, lines 15-39 as above and col. 4, lines 14-22; the inputs are the external device and the first memory area, the outputs are the banks of the IEM; this crossbar encompasses the read address signals); and, a second Address Generation Unit providing Write address data to the second unidirectional crossbar (Dakhil, col. 2, lines 15-39 as above and col. 4, lines 14-22; the inputs are the banks of the IEM, the outputs are the external device and the first memory area; this crossbar encompasses the write address signals).

33. Consider claim 22, Van Hook discloses the FPE further comprises: a plurality of floating point operation execution units (Bishop discloses in page 5 of floating point units).

34. Consider claim 23, Van Hook as modified by Bishop discloses the plurality of floating point execution units are selectively grouped together to form a vector floating point unit (Bishop discloses in page 5 of floating point units; Van Hook in col. 16, lines 7-9, of vector operation).

35. Consider claim 26, Van Hook discloses a first Application Programming Interface (API) associated with the main game program (col. 13, lines 13-16, software architecture/constructs to implement video game program 108 in a high level software environment); and a second API associated with the PPU driver (see, for example, col. 8, lines 39-46, commands which control the coprocessor; also see col. 13, lines 9-16, drivers).

36. Consider claim 27, Van Hook discloses the second API is callable by the first API (col. 13, lines 13-16, software architecture/constructs to implement video game program 108 in a high level software environment; see, for example, col. 8, lines 39-46, commands which control the coprocessor; also see col. 13, lines 9-16, drivers).

37. Consider claim 29, Van Hook as modified by Bishop discloses of a dedicated vector processor adapted to perform parallel floating point operations (Bishop discloses in page 5 of floating point units; Van Hook in col. 16, lines 7-9 discloses of vector operation).

38. Consider claim 30, Van Hook discloses the PPU further comprises a high-speed memory (Figure 5, RDRAM 200).

39. Consider claim 34, Van Hook discloses the general purpose microprocessor generates a command in response to execution of the game program and communicates the command to the PPU (see, for example, col. 8, lines 39-46, commands which control the coprocessor; also see col. 13, lines 9-16, drivers).

40. Consider claims 38-40, Van Hook as modified by Bishop discloses the PCE is configured to call microcode routine (col. 8, lines 53-56, signal processor executes microcode to perform various graphics and audio functions) executed on the DME and FPE (col. 18, lines 11-13, execution unit is managed by instruction memory 402; col. 19, lines 41-44 discloses that the signal processor can transfer data into and out of instruction memory 402 and data memory 404 via DMA; col. 11, lines 65-67 discloses that the signal processor executes the microcode out of the instruction memory 402; thus it is issuing commands to the execution unit. In other words, the microcode routines executed by the signal processor cause both the DME and FPE to perform various functions. Note that one definition of on is "with respect or regard to (used to indicate the object of an action directed against or toward)") to perform physics simulation computations (Bishop, Figure 1, ideal SPARTA implementation; section 1 discloses of physical modeling of solid objects through the use of specialized hardware;

section 2 and section 3.1 discloses of collision detection and force computation, as above).

41. Claims 5, 32-33, and 35-36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Van Hook, Bishop, and Dakhil as applied to claim 1, 31, and 34 above, and further in view of Intel (Intel PCI and PCI Express; note that the subject matter relied upon in the reference is dated).

42. Consider claim 5, Van Hook does not disclose that the CPU and PPU communicate via at least one selected from a group of physical interfaces consisting of: Universal Serial Bus (USB), USB2, Firewire, Peripheral Component Interconnect (PCI), Peripheral Component Interconnect Extended (PCI-X), PCI-Express, and Ethernet.

On the other hand, Intel discloses of a PCI interface, or alternatively, of a PCI-Express interface (pages 2-3, PCI, PCI Express).

The PCI interface is a tenfold performance gain over ISA, has plug-and-play capabilities, and is processor agnostic and flexible (Intel, page 2). Alternatively, the PCI-Express interface supports important features such as power management and the ability to handl both host-directed and peer-to-peer data transfers (Intel, page 3).

It would have been obvious to one of ordinary skill in the art at the time of the invention to implement a PCI interface, or alternatively, a PCI-Express interface, for the above reasons. Alternatively, one rationale that may be used to support the conclusion of obviousness is simple substitution of one known element for another to obtain

predictable results, and it is noted in Figure 2 of Van Hook as modified by Bishop that there exists a bus that connects the CPU and the PPU.

43. Consider claim 32, Van Hook does not disclose that the PPU is operatively connected within the PC by means of an expansion board.

On the other hand, Intel discloses of a PCI interface, or alternatively, of a PCI-Express interface (pages 2-3, PCI, PCI Express). Moreover, it would have been readily recognized to one of ordinary skill in the art at the time of the invention that a device that connects to a PCI interface is an expansion board.

The PCI interface is a tenfold performance gain over ISA, has plug-and-play capabilities, and is processor agnostic and flexible (Intel, page 2). Alternatively, the PCI-Express interface supports important features such as power management and the ability to handle both host-directed and peer-to-peer data transfers (Intel, page 3).

It would have been obvious to one of ordinary skill in the art at the time of the invention to implement a PCI interface, or alternatively, a PCI-Express interface, for the above reasons. Alternatively, one rationale that may be used to support the conclusion of obviousness is simple substitution of one known element for another to obtain predictable results, and it is noted in Figure 2 of Van Hook as modified by Bishop that there exists a bus that connects the CPU and the PPU.

44. Consider claim 33, Van Hook discloses a Graphics Processing Unit (GPU) adapted to compute graphics data for incorporation within execution of the game program (Van Hook, Figure 5, SP 400 or display processor 500).

45. Consider claim 35, Van Hook does not disclose that the PPU and general purpose microprocessor communicate via at least one selected from a group of physical interfaces consisting of: Universal Serial Bus (USB), USB2, Firewire, Peripheral Component Interconnect (PCI), Peripheral Component Interconnect Extended (PCI-X), PCI-Express, and Ethernet.

On the other hand, Intel discloses of a PCI interface, or alternatively, of a PCI-Express interface (pages 2-3, PCI, PCI Express).

The PCI interface is a tenfold performance gain over ISA, has plug-and-play capabilities, and is processor agnostic and flexible (Intel, page 2). Alternatively, the PCI-Express interface supports important features such as power management and the ability to handl both host-directed and peer-to-peer data transfers (Intel, page 3).

It would have been obvious to one of ordinary skill in the art at the time of the invention to implement a PCI interface, or alternatively, a PCI-Express interface, for the above reasons. Alternatively, one rationale that may be used to support the conclusion of obviousness is simple substitution of one known element for another to obtain predictable results, and it is noted in Figure 2 of Van Hook as modified by Bishop that there exists a bus that connects the CPU and the PPU.

46. Consider claim 36, Van Hook discloses the PPU comprises a vector processor adapted to run parallel floating point operations (Bishop discloses in page 5 of floating point units; Van Hook in col. 18, lines 8-11, discloses of execution units responsive to instructions residing instruction memory and of vector operation in col. 16, lines 7-9).

47. Claims 24 and 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Van Hook and Bishop and Dahkil as applied to claim 23 and 34 above, and further in view of Shiell et al. (Shiell) (6317820).

48. Consider claim 24, Van Hook and Bishop do not disclose the FPE performs floating point operations in response to a Very Long Instruction Word (VLIW).

On the other hand, Shiell does disclose of VLIW instructions (col. 1, lines 50-62, VLIW word, a number of different instruction streams are statically scheduled together).

VLIWs are highly effective for regular, loop-oriented tasks such as are typical of the performance-sensitive aspects of digital signal processing and other "number-crunching" applications (Shiell, col. 1, lines 40-43). Furthermore, it would have been readily recognized to one of ordinary skill in the art at the time of the invention that VLIW CPUs offer significantly more computational power, thus increasing system performance.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teaching of Shiell with the invention of Van Hook and Bishop in order to increase system performance.

49. Consider claim 37, Van Hook and Bishop and Dakhil do not disclose the command is a Very Long Instruction Word (VLIW).

On the other hand, Shiell does disclose of VLIW instructions (col. 1, lines 50-62, VLIW word, a number of different instruction streams are statically scheduled together).

VLIWs are highly effective for regular, loop-oriented tasks such as are typical of the performance-sensitive aspects of digital signal processing and other "number-crunching" applications (Shiell, col. 1, lines 40-43). Furthermore, it would have been readily recognized to one of ordinary skill in the art at the time of the invention that VLIW CPUs offer significantly more computational power, thus increasing system performance.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teaching of Shiell with the invention of Van Hook and Bishop in order to increase system performance.

50. Claim 28 is rejected under 35 U.S.C. 103(a) as being unpatentable over Van Hook and Bishop and Dahkil as applied to claim 27 above, and further in view of Telekinesys (Havok Game Dynamics SDK; note that although this particular reference is dated 2002, the base Havok platform predates this reference).

51. Consider claim 28, Van Hook discloses a Graphics Processor Unit (GPU), wherein the host further stores: a GPU driver and a third API associated with the GPU driver (Van Hook, col. 8, lines 39-46, commands which control the coprocessor; also

see col. 13, lines 9-16, drivers) wherein the second API would be callable by the first API (see claim 27 above).

Although Bishop discloses that the Sparta can be integrated with graphics hardware (section 3.4, bullet point 3), based on which examiner believes it would have been obvious that the second API is callable by the third API, Bishop nevertheless does not explicitly disclose this as he does not elaborate on the term “integrated”.

On the other hand, Telekinesys explicitly discloses that the second API is callable by the third API (see, for example, page 19, section 11, interface to the physics system, industry standard graphics API). Also see the first paragraph of section 11, “the first thing any game developer needs to do when using a physics engine is to interface the physics system to the existing 3d graphics / rendering solution.”

Bishop teaches that integrating the physics co-processor with the graphics hardware avoids a bottleneck between the CPU and graphics hardware (Bishop, section 3.4, bulletpoint 3).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teaching of Telekinesys with the invention of Van Hook and Bishop in order to avoid a bottleneck between the CPU and graphics hardware.

Response to Arguments

52. Applicant states on page 10 that examiner cites the CPU interface for teaching of a PCE. However, examiner had cited the signal processor in tandem with the CPU

interface to teach of the PCE (in view of Bishop), and not merely of the CPU interface. Applicant argues that Van Hook does not mention that the CPU interface communicates with the CPU via a PPU driver. While this argument is moot given the use of the signal processor to teach an aspect of the PCE, examiner notes that the claims use the limitation "receive" rather than "communicate."

53. Applicant argues on page 11 that Van Hook does not mention that the execution unit outputs control signals to the display processor. However, examiner had not put forth this interpretation. Rather, examiner noted that the claimed limitation was met either by the signal processor outputting commands to the execution unit, or the signal processor outputting commands to the display processor. Nevertheless, Van Hook teaches in col. 18, lines 8-36, that the execution unit controls the scalar unit, which controls the load/store block which, seen in Figure 7, stores into the display processor commands portion of the data memory 404, wherein the commands are sent to the display processor as per col. 16, lines 44-54.

54. Applicant argues on page 11 that the claim recites a single system element (PCE) that is configured to perform two operations, whereas examiner cites two different system components to teach functionality equivalent to the functionality of the PCE. However, examiner first notes that a PPU "control engine” is sufficiently broad such that it would be feasible that two system components that are directly connected to each other could collectively be considered a “control engine,” just as a “control engine”

in the instant invention is comprised of different modules or components itself. Nevertheless, examiner notes that the signal processor by itself teaches both receiving physics simulation requests from the CPU (col. 8, lines 39-46 and 54-57, col. 9, lines 1-2 for example, commands which control the coprocessor; these commands are processed by the signal processor as cited above) and issue commands to the DME and FPE, as cited in the paragraph above.

Conclusion

55. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The prior art below describe different facets of the Cell Processor and are particularly pertinent; to further prosecution, examiner recommends that applicant convey the main distinctions between the Cell processor and the instant invention in reference to the current set of claims.

n. Suzuoki et al. (US 20020156993) discloses of a similar architecture to the instant invention (e.g. a PU controlling an APU in an analogous manner as the instant invention's CPU controlling the PPU).

o. Altman et al. (US 6779049) discloses of APUs access to shared memory.

p. Gschwind et al. (US 20040083342) discloses of a memory flow controller in the APU/MPU environment

q. Kahle (US 20040193754) discloses of a memory flow controller in the context of a synergistic processing unit.

56. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

57. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Keith Vicary whose telephone number is (571)270-1314. The examiner can normally be reached on Monday - Thursday, 7:00 a.m. - 5:30 p.m., EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on 571-272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Keith Vicary/
Examiner, Art Unit 2183

/David J. Huisman/
Primary Examiner, Art Unit 2183